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TWO CHEAP, TEMPERATURE STABLE, BATTERY-OPERATED DEVICES PRODUCING A CURRENT LINEARLY PROPORTIONAL TO CAPACITANCE OR RESISTANCE

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INTRODUCTION

It is becoming common for ecologists to measure water level or water content by a capacitative method. In a simple case water rises or falls between two metal plates, one at least of which is insulated. The dielectric constant of water (about 80) is much greater than that of air (about 1), so the capacitance between the plates is nearly proportional to the water level. Design criteria are discussed by Wilner (1960).

The measurement of capacitance in field conditions requires a device which is accurate and reliable over a wide temperature range. It should operate from a low voltage supply and use little current. Because ecologists need—or at least they often want—to make measurements at several points and to have these recorded automatically, the device should be cheap and should allow the sensor and recorder to be earthed. To avoid a multiplicity of batteries and voltage stabilizers the power supply should also be earthed. It is desirable to be able to offset stray capacitance in the sensor cable and useful if the output is a linear function of capacitance. Computer processing can nowadays cope easily with non-linear responses but non-linearity must still give variation in accuracy and precision.

So far as we know, this combination of properties—cheapness, reliability, linearity, low power consumption, low voltage, temperature stability, zero offset and common earthing of power supply, capacitor and meter—is not possessed by any published design. The recent development of integrated circuit (IC) complementary metal oxide silicon (COS/MOS) devices has now made such designs possible. These have considerable advantages over bridge circuits, including Lion's (1964) non-linear twin-T, and over the usual resistor-capacitor delay circuits. A single IC contains four gates or six inverters and costs about £0·5.

Two such designs are described here.

DESIGN A

The principle is shown in Fig. 1. The variable capacitor C1 charges rapidly through the diode D1, but discharges more slowly, through resistor R1. The inverter output has two voltage levels, zero and V_{dd}. It switches very rapidly from one to the other when the input voltage passes through the transition voltage V_t. The inverter I1 acts simply as a switch which is turned off at the same time in each cycle by the sharp rise in the oscillator output, but which is turned on (when the input reaches V_t) after a delay proportional to the capacitance C1. The time during which the output is high is linearly proportional to capacitance. So, therefore, is the average output current, which is measured by the meter

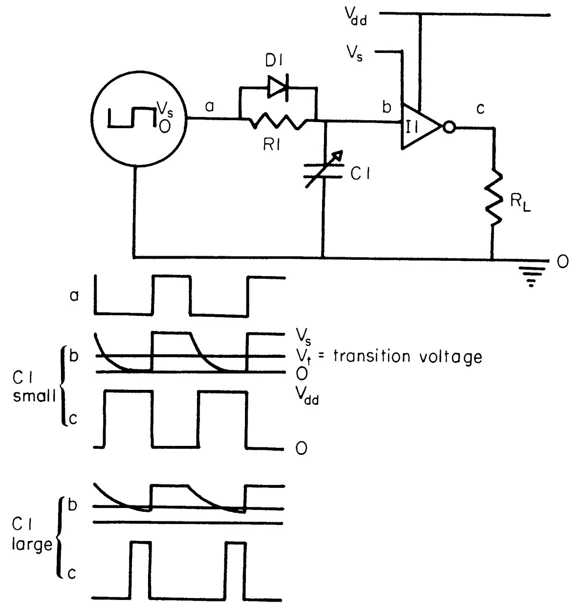

FIG. 1. Basic circuit and idealized waveforms for design A.

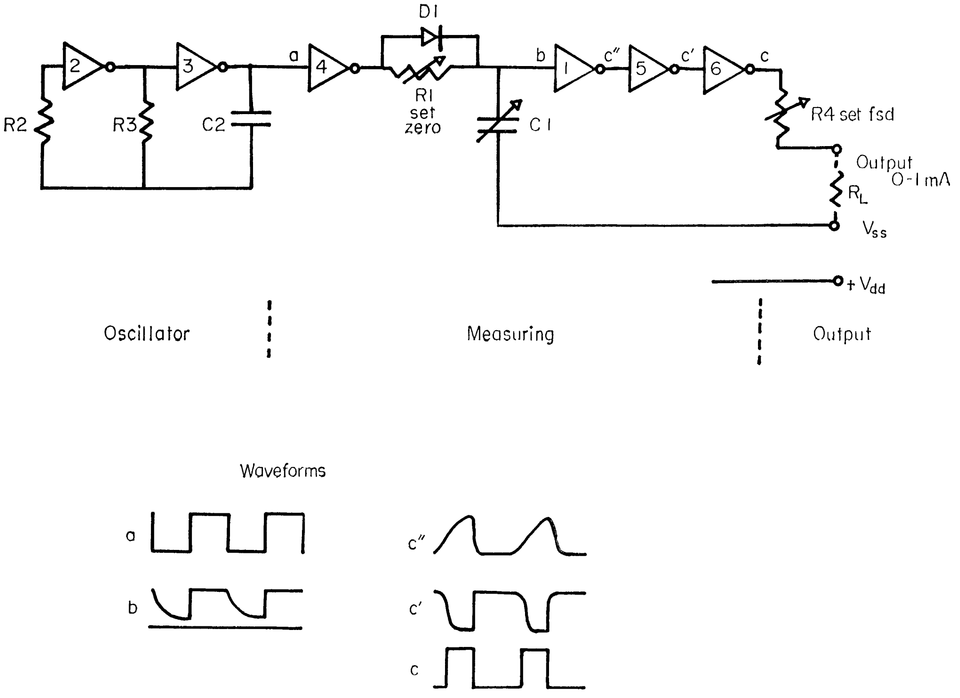

FIG. 2. Practical circuit and waveforms for design A. The output across R_L is a linear function of the capacitance C1.

of resistance R_L. The main difficulty in implementing this principle is to find an inverter whose V_t is little affected by temperature. COS/MOS devices have this property.

A practical version is shown in Fig. 2. Inverters 2 and 3 with R2, R3 and C2 form an oscillator (Anon. 1971) producing a rectangular wave with mark:space ratio about 1:1. The repetition rate is determined by the product R3 × C2. Inverter 4 acts as a buffer protecting the oscillator from the measuring section. The inverters 1, 5 and 6 connected in series produce a wave form close to the ideal shape shown for I1 in Fig. 1. The individual inverter transfer characteristic (Fig. 3) is far from ideal (in the applications for which the available inverter is designed there is no need for a close approach to the ideal) but three inverters in series are sufficient to convert the capacitor discharge curve at b (Fig. 2) through c″ and c′ to the rectangular form at c. The inverters can supply 1 mA at output without significantly reducing the voltage below V_{dd}. If the power supply voltage can be kept stable a simple resistor R4 can be used to control the full scale deflection (fsd) of the meter.

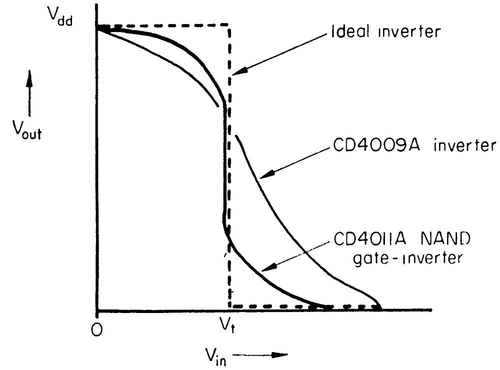

FIG. 3. Inverter and gate-inverter transfer characteristics: ideal and actual.

In use one sets C1 at maximum, then adjusts R1 to give zero meter reading. Then C1 is set to minimum and R4 is adjusted to give fsd. The meter scale must be calibrated backwards, but stray capacitance in cables is 'offset' beyond fsd.

The device may be remote from power supply and meter. Only three connections, one of them earthed, are needed.

The choice of values for resistors and capacitors starts from the oscillator. Repetition rate is decided, bearing in mind the high harmonic content of rectangular waves. The value of C2 should be between about 33 and 10 000 pF. Repetition rate is approximately 1/(2·4 × R3 × C1) and R2 should be at least double R3. When C1 is maximum R1 is about 0·75 × R3 × C2/C1, but if R1 is less than about 4 kΩ the output may be more temperature sensitive and less linear. The supply voltage V_{dd} should be between 5 and 15 V, the higher values being preferable for high repetition rates, and R4 is then $V_{dd}/I_m - R_L$ kΩ (R_L in kΩ; I_m, the average output current, in mA).

To ensure a stable repetition rate the oscillator components should be physically close together and should have small temperature coefficients. Tin oxide resistors and polystyrene capacitors were used in tests. The zero and fsd controls (R1 and R4) should also have small temperature coefficients. 'Cermet' potentiometers are suitable, but at £0·9 each account for two-thirds of the total cost. If the device is dedicated to one sensor and used with only one particular meter then R1 and R4 can be fixed. The whole device (excluding power supply and meter) then consists of one IC (containing six inverters), one capacitor, one diode and four resistors. It can be packed in a space 2·4 × 1 × 1 cm and costs less than £1. If the ratio mark: (mark + space) when C1 is set to minimum is s, then the current i_m from the inverter when it is on is I_m/s. If i_m exceeds about 20 mA then the output resistance of the inverter rises and this affects linearity and stability. In practice, therefore, s at minimum C1 should be at least 0·05 and this limits the proportion of C1 which can be offset.

This circuit uses about 20 mA. Charging of C1 through D1 is not instantaneous and causes the voltage rise to b (Fig. 1) to be slightly curved. At high repetition rates this causes non-linearity at the higher values of C1.

DESIGN B

The second design uses less current, retains linearity at higher repetition rates, has greater temperature stability than design A and allows more of C1 to be offset. But it costs about £1 more.

The principle is shown in Fig. 4. The output from a rectangular wave generator is divided. Part goes direct to an AND gate. The output voltage from this gate switches very rapidly from zero to V_{dd} but only when both inputs exceed the transition voltage V_t. The other part of the oscillator output is delayed in reaching the gate by R1*C1, as in design A. The length of the pulses from the gate is therefore linearly proportional to C1 and so also is the average output current. The gate is closed at the same position in each cycle by the voltage fall in the original wave form, but is opened only after a delay proportional to C1. Gate closing is faster than in design A and higher repetition rates can therefore be used. The voltage transfer characteristics of COS/MOS gates are nearly ideal over 40% of V_{out} (Fig. 3) and V_t of the gates is less affected by temperature than it is for the inverters.

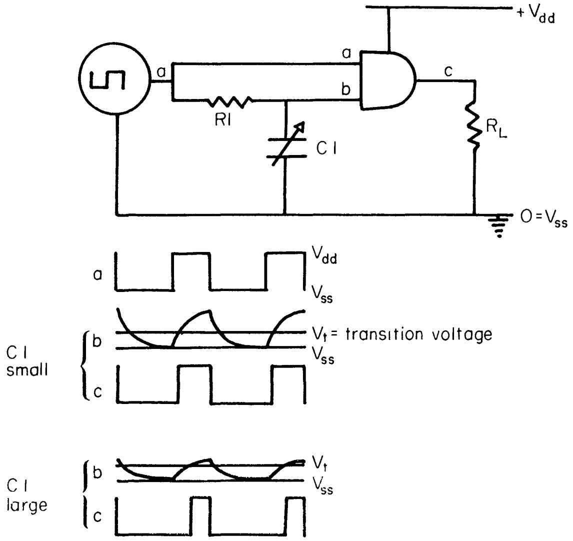

FIG. 4. Basic circuit and idealized waveforms for design B.

Because the capacitor C1 in Fig. 4 both charges and discharges through R1 the mark space ratio must be less than 1:1. This restriction is removed in the practical circuit shown in Fig. 5 by using a diode D1 which allows C1 to discharge rapidly. Note, though, that one does not rely on this to close the gate-inverter 7. The gate-inverters 1, 2, 5, 6 and 8 are used simply as inverters, 3 and 4 are buffers. A single IC contains 4 NAND (AND gate with inverter) 2 input gate-inverters. One is essential for gate 7, so the other three are used as inverters or buffers. Another IC provides the other four inverters.

The oscillator is the same as that of design A. Gate-inverters 3 and 4 act as buffers. Gate-inverters 5 and 6 are used, as were the inverters in design A, to convert the capacitor-charging curve of b″ to a rectangular wave at b. Because of the better transfer characteristics only two gate-inverters are needed. Gate-inverter 8 re-inverts the output from 7, so that the full meter scale may be used with one terminal grounded.

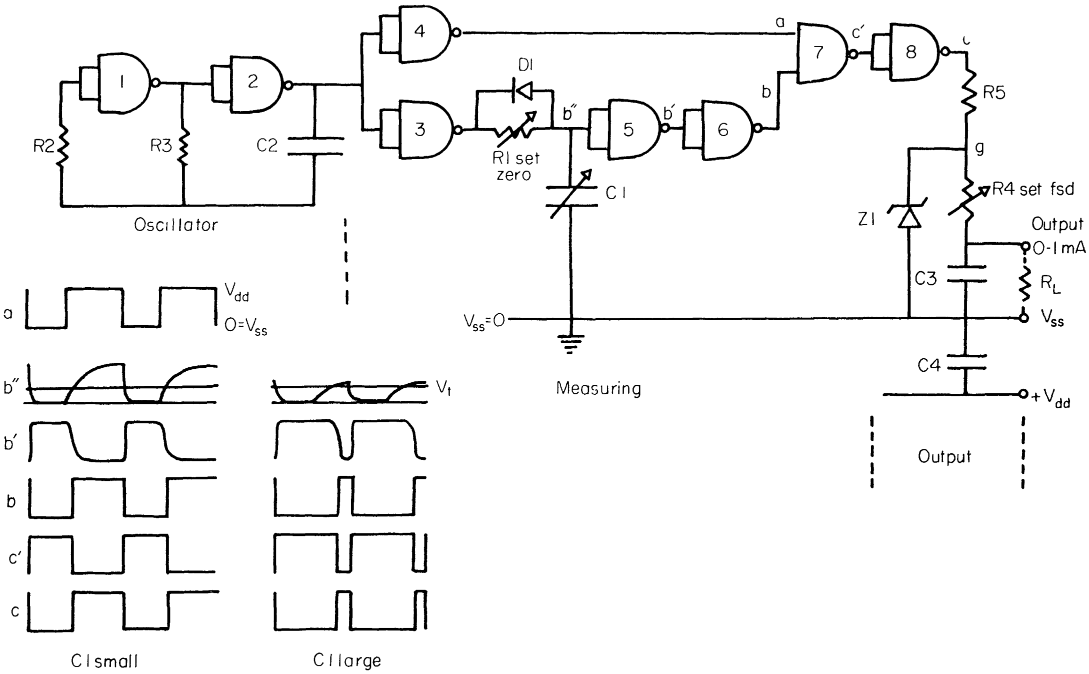

FIG. 5. Practical circuit and waveforms for design B. The output across R_L is a linear function of the capacitance C1.

The NAND gates show a reduction in output voltage at smaller output current than do the inverters of design A: 1 mA may cause significant non-linearity. To deal with this problem and to provide some independence of supply voltage, the zener diode Z1 is used to clamp the voltage to V_z at g. The value of Z1 is chosen to have a small temperature coefficient—usually about 5·6 V. The resistor R5 limits the current and R4 is used as in design A to set fsd. The decoupling capacitors, C3 and C4 are a further refinement. Zero and fsd are set as they are in design A.

Values of resistors and capacitors in the oscillator and measuring sections are chosen as they were in design A. The supply V_{dd} is chosen as in design A. Then R5 and R4 are calculated. The current while the gate is open, i_g, should not exceed 8 mA. The Zener-diode current, i_z, should be about 3 mA. The *average* meter current, I_m, is 1 mA. If the ratio mark:(mark+space) at fsd is s then the meter current while the gate is open, i_m, is

I_m/s. (Since $i_g = i_z + i_m$ then i_m can be up to 5 mA, and for $I_m = 1$ mA the mark:space ratio can fall as low as 0·2. For very small C1, s approaches 0·5, so that up to 60% may be offset.) The output resistance of the gate, R_c, is about 0·4 kΩ up to 8 mA current drain. Hence,

$$R5 = (V_{dd} - V_z)/(i_z + I_m/s) - R_c$$

and

$$R4 = s\, V_z/I_m - R_L.$$

The decoupling capacitors C3 and C4 are about 47nF and are mounted with the other components. Power supply and meter may be some distance away and only three connections, one of them earthed, are needed. The output voltage is integrated by C3, so the cable carries only DC and may be as long as desired. Current consumption is about 5 mA.

The component cost of the device (excluding the meter) is about £3.50 or £1.50 if R1 and R4 are fixed.

The output section of this design could, of course, be used with design A.

The average meter current, I_m, may be increased without exceeding design limits by increasing the oscillator mark-space ratio. This may be done by replacing R3 by a pair of resistors in series, and shunting one with a diode. A Schmitt trigger input COS/MOS gate and an inverter with gate characteristics should soon be available. These should allow designs with slightly improved performance.

Table 1. *Design B: deviations from linearity, expressed as %fsd, with change in supply voltage and temperature; repetition rate* 25 *kHz; zero and fsd set for supply* 12·2 *V*

Supply (V)	Capacitance (pF) Temperature (° C)	0	50	100	150	200	250
11	−22	−1·5	−1	+0·5	+1	+2·5	+3
	25·5	0	+1	1·5	+2·5	+3	+2·5
	50·5	−1	+1	+2	+2	+3	+2·5
12	−22	−1·5	−1·5	0	0	+1	+1
	25·5	0	−0·5	+1	+1	+1	+0·5
	50·5	0	+0·5	+1	+1·5	+1	+1
14	−22	−3	−2	−1·5	−1·5	−1·5	−1*
	25	−0·5	0	0	−1	−1·5	−1·5*
	50·5	0	+0·5	+0·5	0	−1	−1·5*

* Estimated by extrapolation: zero output at less than 250 pF.

TESTS

In all tests the capacitor C1 was kept at room temperature (24–27° C). The first tests were made with design B. The effects of variation in power supply voltage and in temperature were measured. Then the oscillator repetition rate was varied. Some components were unchanged in all tests.

Component	Type/value	(Supplier)	
NAND Gates 1–4	*CM 4011AE	(Solitron)	4 ICs permuted and the pair giving largest deviations from linearity used.
NAND Gates 5–8	CM 4011AE	(Solitron)	
D1	1N4148	(RS)	

* Alternative devices are: R.C.A. CD4011AE, National Semiconductor MM 4611A.

Table 2. *Design B: deviations from linearity, expressed as % fsd, with change in repetition rate and temperature; zero and fsd reset at about 27° C for each repetition rate;* 14·2 *V supply; cable capacitance* 180 *pF*

Repetition rate	R3	C2	Maximum current to device	Maximum current at output	temperature	C1 capacitance (pF)					
kHz	kΩ	pF	mA	mA	° C	0	50	100	150	200	250
1·07	380	1000	2·8	1·16	26·5	+ 0*	+0·1	+0·3	+0·2	+0·5	0*
	(R1 = 1·2M)				−22	+0·5	+0·8	+0·8	+0·6	+0·1	+0·6
25	33	470	3·0	1·17	26·5	0*	+0·8	+0·8	+0·6	0	0*
					−21·5	−0·8	+0·2	+0·8	+1·2	+1·4	+0·8
86	33	100	3·4	1·18	26·5	0*	+0·2	+0·8	+0·4	+0·4	0*
					−22	0	+0·8	+1·4	+1·2	+1·0	+1·0
145	33	47	4·4	1·19	27	0*	0	0	0	−0·2	0*
					−22	0	0	−0·2	−1·0	−1·0	(−1·5) (estimated)

* Set points.

Table 3. *Design A: deviations from linearity, expressed as %fsd, with change in repetition rate and temperature; zero and fsd reset at about 25° C for each repetition rate; regulated power supply (TO5) 14·2 V; cable capacitance 260 pF*

Repetition rate kHz	R3 kΩ	C2 pF	Temperature ° C TO5	Circuit A	Current to device mA	0	50	100	150	200	250
3·3	33	4700	28	28	19·8	0*	−0·9	−1·2	−0·8	0	0*
			−22	−22		+1·8	+1·8	+2·0	+1·4	+2·2	+2·8
27	33	470	24	24	19·6	0*	−0·2	−0·3	−0·2	0*	+1·0
			−22	−22		+2·0	+2·0	+1·8	+1·8	+2	+0·8
			25	−22		+1·8	+1·8	+1·3	+1·5	+1·8	+0·6
			−22	25·5		+0·1	+0·2	+0·2	+0·2	+0·1	+0·8
143	33	47	25·5	25·5	19·4	0*	+0·2	+0·2	−0·8	−0·8	0*
			−22	−22		+3·0	+2·8	+2·2	+1·2	+0·4	+0·0

* Set points.

Z1	5·6 V	(RS)
R1	50 kΩ Cermet	(RS)
R4	2 kΩ Cermet	(RS)
R5	1 kΩ tin oxide	(RS)
C3, C4	47 nF ceramic	(RS)
R_L	Mk VIII Avometer 1 mA DC range	
C1	0–250 pF precision rotary capacitor	

In the first tests the oscillator was run at 25 kHz using:

R2	68 kΩ tin oxide (RS)
R3	33 kΩ
C2	470 pF polystyrene (RS).

Zerò and fsd were set using a 12·2 V supply. The effects of varying supply voltage and temperature are shown in Table 1.

It seems clear that supply voltage can usefully be stabilized. Any value between 10 and 15 V gives acceptable results, but the higher value is better if the oscillator repetition rate is high. In the next tests (Table 2), V_{dd} was fixed at 14·2 V and repetition rate varied. The linearity and stability between 1 and 145 kHz, and between −22 and +27° C are adequate for most ecological purposes.

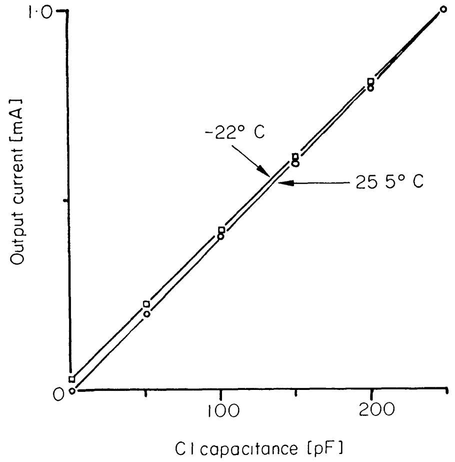

FIG. 6. Output current as a function of capacitance C1, design A, 143 kHz. This was the worst case in tests.

These tests were made using a mains-driven variable voltage supply. In field conditions voltage control may be more difficult. A simple Zener controlled supply proved insufficiently stable, but an IC controller (RS type T05, Signetics μA723) set to provide 14·2 V was stable ±0·05 V over the temperature range −22 to +51° C. The TO5 consumed about 4 mA. The cost is about £1.50, and a single controller can supply many measuring devices. A supply of 16·5 to 40 V is necessary; 24 or 27 V is convenient and allows batteries to be run for a large part of their useful life. This controller, with a 20 V supply, was used to test design A (which relies on a stable power supply). Both controller and device were tested at −22 and +26° C at three repetition rates. The results are shown in Table 3. The measurements at 27 kHz show that changes in output with temperature are not caused by the power supply. In general, non-linearity and drift are up to 3% of fsd, but these large deviations occur at high repetition rate and high values of capacitance C1. At low repetition rates and over a restricted range of temperature this design may be satisfactory. The *worst* case, 143 kHz, is shown in Fig. 6.

The tests have all been made with the output as a function of capacitance. There is no reason why the same circuit should not be used for measuring resistance at R1 using fixed C1. The measurement of resistance is not usually difficult, however, and the practical restriction of the use of this design to values greater than about 4 kΩ gives it few attractions for this purpose.

SUMMARY

Two devices are described which may be used to measure capacitance or resistance in the field. The devices should be particularly useful in measuring water content or water level. One device is linear to about ±1% over the temperature range −22 to +51° C and for repetition rates from 1 to 140 kHz at least. Output is from 0–1 mA (average) and current consumption is less than 5 mA. Battery, capacitor and meter are all earthed. Cable capacitance may be offset. This device costs less than £4.

The second device is simpler, takes about 20 mA, can cost less than £1, but is more non-linear (±2%).

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