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A low latency multichannel audio processing evaluation platform

Yonghao Wang[1], Xiangyu Zhu[2], and Qiang Fu[3]

[1] Queen Mary University of London, Centre for Digital Music London, E1 4NS, UK
yonghao.wang@eecs.qmul.ac.uk
and Birmingham City University, Birmingham, B4 7XG, UK
yonghao.wang@bcu.ac.uk

[2] Hebei University of Science and Technology, Shijiazhuang, 050018, P.R.China
xiangyu-zhu@hotmail.com

[3] Shijiazhuang Mechanical Engineering College Shijiazhuang 050003, P,R,China
asajapa@sina.com

ABSTRACT

For live digital audio systems with high-resolution multichannel functionalities, it is desirable to have accurate latency control and estimation over all the stages of digital audio processing chain. The evaluation system we designed supports 12 channel, 24 bits Sigma Delta based ADC/DAC, incorporating both a programmable FPGA and a Digital Signal Processor. It can be used for testing and evaluation of different ADC/DAC digital filter architectures, audio sample buffer subsystem design, interrupt and scheduling, high level audio processing algorithm and other system factors, which might cause the latency effects. It also can estimate the synchronization and delay of multiple channels.

1. INTRODUCTION

In real time audio systems, latency is a well known problem [1]. It limits the range of applications and causes some undesirable delay effects for multiple channels such as comb filter effects [2][3][4]. For live dubbing processing latency of more than few milliseconds will cause discomfort [5]. For software synthesizers and electronic music instruments, the engineer would like the latency at a sub-millisecond level [6].

In recent years, software digital audio workstation (DAW) based live systems have become increasingly popular in live performance environments. However, latency is always a concern when the standard computer system is used as a platform for live DAWs [7][8][9].

Most dedicated live systems, such as live music or broadcast consoles, have specific design considerations in both hardware and software architectures [10].

In order to reduce the system latency, it would be useful to evaluate and investigate the latency of different stages such as I/O, ADC/DAC [11], buffer setting, scheduler [12] and the DSP algorithms [13] to identify the components contributing most latency, the cause of the latency and the possible solutions.

Therefore this paper proposes a DSP and FPGA based multichannel audio processing latency evaluation system, which could provide an effective test bed for evaluating the latency problem. A first version of hardware prototype has been made. The platform is depicted in Figure 1.

Figure 1 Hardware realisation of the low latency multichannel audio processing evaluation platform

2. LOW LATENCY MULTICHANNEL AUDIO PROCESSING EVALUATION PLATFORM

2.1. General Architecture

The system block diagram is shown in Figure 2. It consists of three main parts:

1) The Inputs/Output (I/O) block contains 12 channels sigma delta (ΔΣ) based ADC/DACs.

2) The FPGA is used for post-processing Direct Stream Digital (DSD) or Pulse-Code Modulation (PCM) sampled data.

3) A digital signal processor (DSP) for implementing general real-time DSP algorithms.

In addition, the platform has auxiliary modules, Ethernet ports, and onboard Flash and SDRAM memories. It is mainly designed for multichannel audio signal low latency processing or latency measurement. The detailed functionalities are discussed in Section 3.

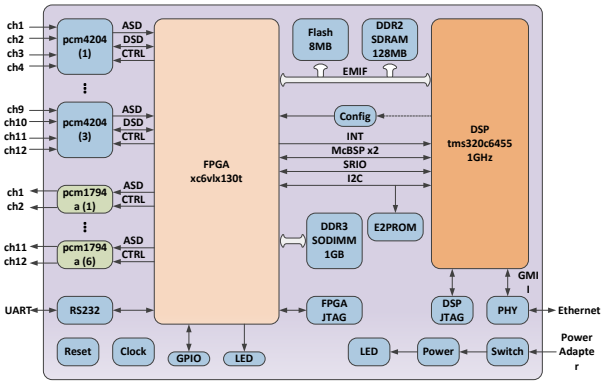

Figure 2 Block diagram of the Platform

2.2. Main Features

The board has the following major features:

- 12 channels of Delta-Sigma ADC: 24-bit resolution, 192kHz sampling, Dynamic Range: 118dB, THD+N: −105dB, support Linear PCM Output through Audio Serial Port and Direct Stream Digital (DSD) Output through DSD Data Port.

- 12 channels of Sigma-Delta DAC: 24-bit resolution, 192kHz sampling, advanced segment, Dynamic Range: 127 dB, THD+N: −108dB，support external digital filter.

- Virtex-6 FPGA in the data path between ADC/DAC and DSP, with a SODIMM type DDR3 SDRAM expansion slot. 1 GB DDR3 SDRAM mounted.

- TI TMS320C6455 DSP running at 1GHz, with external 128MB DDR2 SDRAM, 8MB Flash, 64Kb I2C serial EEPROM.

- 1000Mbps Ethernet supported by the DSP.

- EMIF, McBSP x2, SRIO and I2C buses available for data transmission between FPGA and DSP. 4 INT

signals used by FPGA to trigger interrupting routine of the DSP.

- 16 GPIOs, 4 LEDs and 1 RS232 UART supported by FPGA and accessible by the DSP.

- FPGA configuration is controllable by the DSP.

2.3. Interfaces

Interfaces of the platform are shown in Table1. The FPGA also provide facilities to enable future digital interfaces to be incorporated such as SPDIF or AES10.

Interfaces	Amount	Description
ADC	12	(a)
DAC	12	(b)
Ethernet	1	(c)
UART	1	(d)
GPIO	16	(e)
DSP JTAG	1	(f)
FPGA JTAG	1	(g)
Power Adapter	1	(h)

Table 1 Interfaces

Details of the interfaces are as follows;

(a): Delta-Sigma ADC, 24-bit resolution, 192kHz sampling, Dynamic Range: 118dB, THD+N: −105dB.

(b): Sigma-Delta DAC, 24-bit resolution, 192kHz sampling, Dynamic Range: 127dB, THD+N: −108dB.

(c): 1000Mbps Ethernet.

(d): RS232, provided by FPGA.

(e): 3.3V LVTTL, provided by FPGA.

(f): DSP debugging port.

(g): FPGA configuration and debugging port.

(h): Power supply for the platform.

3. FUNCTIONALITY

3.1. Programmable audio signal processing

This platform has multichannel ADC/DACs, FPGA, and DSP. It is suitable for real-time audio signal processing. Various kinds of software algorithms can be implemented and evaluated on this platform, and different hardware subsystem architectures can be prototyped and evaluated in the FPGA area.

In the general scenario, audio signals are converted from analogue to digital form by a ΔΣ ADC. The FPGA receives the digital signals in DSD or PCM form, and then it can take processing steps such as decimation or sample rate conversion (SRC). The signals are then sent to the DSP for the application of, for example, a specific audio effect. The signals can then return to the FPGA for it to perform some postprocessing such as hardware based filtering or framing. Finally, the FPGA sends the signals to the DAC for conversion back to analogue form. The final analogue signals of the platform can be sent to any receivers, e.g., loudspeakers. The original and the final signal of the platform can be monitored by an oscilloscope for latency measurement and wave comparison.

All data buses in the data path are designed with a sufficiently high clock rate to be able to process the multiplexed audio data without delay. Both FPGA and DSP also run at high clock rates high enough to achieve the theoretical sample based processing. Therefore, low latency multichannel audio signal processing can be investigated.

In the following sections, we discuss the possible real time audio processing research topics that could be supported by this platform.

3.2. Multichannel audio signal capturing, compressing and transmitting

Multichannel audio signal capturing and delivery are common in modern audio applications. There are various digital audio protocols for multiplexing audio channels within the audio system or between audio systems [14][15]. The FPGA components in our platform can be used for prototyping or evaluating different audio multiplexing and transmitting methods. With increasing applications of transmitting professional audio frames in network environments this platform with Gigabits Ethernet port can also be used for generating the required audio frame structure and control messages over different layers of the network including various compressed and uncompressed audio codecs.

3.3. Programmable audio signal generating

The FPGA can be programmed to generate various digital audio signals for research purposes. The DSP can also be programmed to generate digital audio signals. By combining this system with external audio sources, it would be interesting to investigate how hardware (FPGA) can be programmed to allow multiple signal sources to be synchronised in a cooperative manner.

3.4. ADC Decimation Filter evaluation

The ΔΣADCs in the system have Direct Stream Digital (DSD) data ports, which can output 1-bit or few-bit data directly from sigma delta modulator (SDM) [16]. This architecture makes using FPGA to design and evaluate customized digital decimation filters available. In order to evaluate a customized filter, a sine wave source is needed. Data before and after filtering can be stored in a buffer and read by DSP software for latency measurement. This provides a good facility to evaluate different decimation filter architectures such CIC and multistage FIR filters [17].

3.5. DAC Interpolation Filter evaluation

DACs in the system support external interpolation filtering mode. In this mode, the DAC's internal interpolation filter is bypassed, while external interpolation filtering can be performed by FPGA. There has been recent interest to have different interpolation filters rather than linear phase FIR in DAC stages to eliminate pre-ringing [18]. This platform provides good facilities to enable this research.

3.6. Sample Rate Conversion (SRC) evaluation

When different sampling frequencies are supported by different channels, the FPGA can provide real time sample rate conversion (SRC) functionality. Depending on the algorithm of SRC, various latencies caused by this process can be evaluated. Alternatively, it can be configured to send a multichannel signal with different sampling frequencies to the DSP directly to evaluate the software and interface impact in dealing with multiple sampling frequency problems.

3.7. Live intelligent mixer

Moorer [20] has described three stages in the music production development. In the past the audio profession concentrated on "fidelity of reproduction". The main goal was to reproduce the sound accurately as perceived in live concert environments. Currently we are in the "supernatural recording" stage, in which recorded sound is extensively crafted artificially. Based on his extrapolation, in the future, an audio engineer may need to deal with thousands of channels with million points FFT effects in real time. The amount of information is beyond the capability of any proficient audio engineer and necessitates the era of the "intelligent assistant". Thus an intelligent mixer [21] is needed to automate the processes and enable intelligent systems for audio production [22]. Therefore this platform with DSP and FPGA could be used to research the algorithm and architectures needed for intelligent mixing [21].

3.8. Latency measurement

Latency measurement can use cross-correlation delay estimation method, or use a simple method that routes the signals to a mixed signal oscilloscope for manual reading of the latency values. Figure 3 shows an example of buffering latency measurement using a mixed signal oscilloscope. There are multiple testing points designed into the whole signal route. The FPGA is used to implement a BIST (Built-In-Self-Test) [19] module, which incorporates external stimulus and test equipment to be able to measure the latency in different stages and evaluate the delay between different channels.

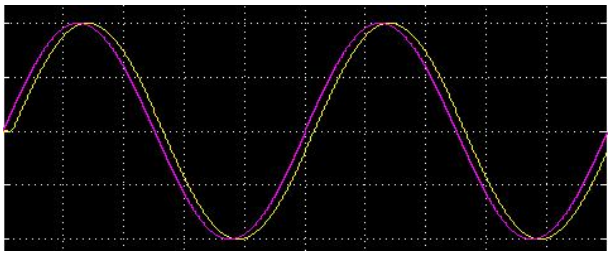

Figure 3 Buffered latency measurement using a mixed signal oscilloscope

This platform can evaluate the latency caused by DSP, ADC/DAC, decimation and interpolation filters, RAM and Buffer, multichannel Audio interfacing and protocols, as well as interrupts, software scheduler, parallel processing and low latency audio processing algorithms. Based on this board, we can explore possible system architectures to support zero buffer or sample based audio processing. It provides a research

platform for further work on optimal minimum latency audio processing systems.

4. CONCLUSION

A low latency multichannel audio processing evaluation system has been designed and implemented to precisely measure and control the signal latency with the support of high level DSP algorithms in either hardware, software or mixed form. The result of this work can be useful for development of improved system architectures, hardware design, software architectures, and algorithm design. It also provides a test bed for evaluating high-resolution audio quality and delay estimation, and synchronization of multiple channels.

The current hardware platform is the first version of the prototype. In the future, the authors would like to further incorporate a multicore CPU architecture with mixed digital signal processor and general-purpose CPU cores in this design in order to apply this research to wider fields.

5. ACKNOWLEDGEMENTS

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